POC-LL a proof of concept of the Parallel Optical computing

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Over the past months, I have been working on a proof-of-concept for a **dual-panel "optical chip" architecture** implemented entirely on an FPGA (Cyclone V / Terasic DE10-Standard).

The goal is not to reproduce the full physics of an optical stack yet, but to validate the **computational architecture** behind a future dual-panel, sensor-array–based optoelectronic processor

What the PoC does

In this prototype:

- The two TFT panels are **emulated as 2D spatial memories** in FPGA block RAM (framebuffers A and B).
- A configurable local **interaction core** computes a virtual optical output $I_{out}(x, y) = f(A(x, y), B(x, y))$.
- A **sensor model** applies gain/offset (and optionally noise) to produce a measurement plane $Y(x, y)$.
- A **ternary classifier** maps each cell into three robust classes (dark, gray, bright), interpreted as a balanced signed-digit alphabet $-1,0,+1$.
- On top of this substrate, I implement:
    - MSD (Most-Significant Digit) arithmetic with multi-frame recoding and normalization.
    - Matrix–vector–like operators with spatially parallel local products and row-wise accumulation.
    - Core **Hyperdimensional Computing (HDC)** primitives (binding, bundling, similarity).
    - A "quantum-inspired" branch workflow in the spirit of teleportation-style spatial coding, with branch duplication, conditional corrections, and high-level control via HDC-like similarity.

All of this runs in real time on the Cyclone V, using the FPGA as a **virtual dual-panel optical processor** with an integrated sensor plane.

Why this matters

This PoC demonstrates three key points:

1. **Reconfigurable substrate**
   The same dual-panel + sensor architecture can be programmed as:
    - an MSD arithmetic engine,
    - a matrix–vector accelerator,
    - an HDC inference engine,
    - or a branch-structured "quantum-inspired" pipeline,
      simply by changing LUTs, spatial patterns, and frame scheduling. This supports the idea of a *general-purpose optoelectronic computing fabric*, not just a single-function optical accelerator.

2. **The sensor as a computational fabric**
   The readout plane is treated as part of the computation, not just as a camera:
   - it applies calibrated gain/offset correction,
   - performs local ternary classification (dark/gray/bright),
   - and feeds directly into MSD/HDC operations.
     This reflects a shift from "imaging" to **distributed measurement and symbol processing**.
3. **Layered computation: MSD + HDC + quantum-inspired coding**
   The same stack supports:
   - **MSD** for local, carry-free multilevel arithmetic and staged normalization,
   - **HDC** for robust, noisy high-dimensional association and similarity,
   - **quantum-inspired spatial coding** for branch creation and correction.
     These are not separate application domains anymore, but **layers on the same dual-panel/sensor substrate**.

Limitations (by design)

At this stage, the PoC is *deliberately* optical-agnostic at device level. It does **not** yet address:

- TFT-LCD response times, thermal drift, pixel non-uniformity, alignment issues.
- Physical phenomena such as diffraction, cross-talk, polarization-dependent aberrations.
- True sensor limitations (dynamic range, fill factor, frame rate, noise texture).

In other words: this is a **proof-of-architecture**, not a proof-of-physics. The focus is on validating representation, scheduling, and the digital control/decoding stack that a future optical chip will need.

Next steps

The roadmap is clear:

- Refine the digital model with more realistic non-linearities, drift and noise.
- Move to a **hybrid bench** with at least one real panel and a real sensor, using the same FPGA backend.
- Progress towards a **physical dual-panel + sensor-array prototype**, where the FPGA logic developed here becomes the native controller of a genuine optical interaction core.

- Benchmark concrete tasks: HDC associative memory, small matrix–vector kernels for AI, and branch-sensitive quantum-inspired workflows.

If you are interested in **hybrid optical–digital architectures**, HDC on spatial substrates, or the intersection between quantum-inspired algorithms and display-based computing, I'd be happy to connect and discuss potential collaborations.